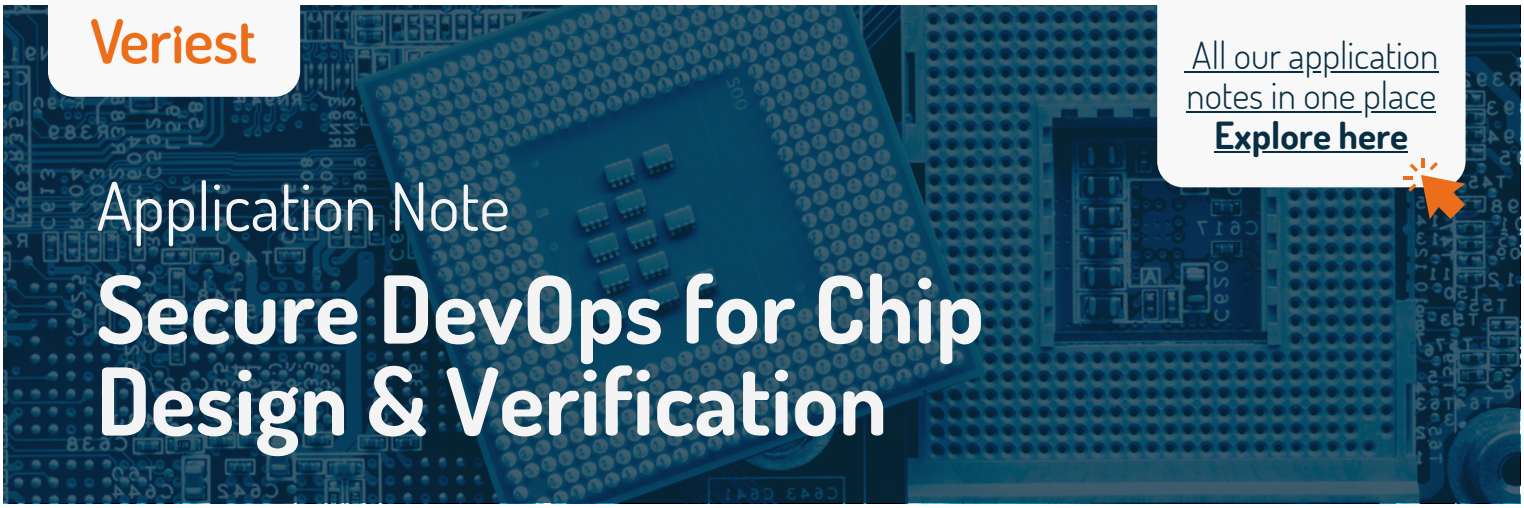
Veriest



All our application notes in one place **Explore here**

Application Note

Secure DevOps for Chip Design & Verification

Traditional Challenges

- The complexity of modern chip design is exploding, leading to verification bottlenecks
- Increased risk of errors and design flaws impacting product quality
- Lack of centralized management for design and verification processes
- Difficulty in ensuring predictable outcomes and meeting project timelines
- Traditional build and test approaches lack automation and traceability

Additional Current Challenges

Security and IP protection concerns with cloud-based solutions

- Data sovereignty and control requirements for sensitive chip designs
- Performance bottlenecks with remote DevOps solutions
- Difficulty integrating with existing on-premises EDA tools and infrastructure
- Compliance with industry regulations for secure development processes

Veriest Solution

Veriest has implemented a comprehensive on-premises DevOps strategy:

- Human-readable, declarative language to define workflows, focusing on what to achieve
- Pre-built workflow templates library that users can customize for specific needs
- Microservices architecture optimized for code compilation, simulation, and testing
- Fine-grained access control and detailed audit trails for accountability
- API-driven workflow execution and webhook support for event-driven processes
- On-premises simulation management to maximize simulation speed and data security
- Customizable workflows that adapt to specific design methodologies

Results

- Enhanced security and IP protection with complete data sovereignty
- Optimized performance with low latency and high-speed simulations on local networks
- Seamless integration with existing EDA tools and infrastructure
- Compliance with stringent industry regulations
- Improved productivity through automated workflows and templates