Veriest

Application Note

PCIe Switch Verification: Challenges and Solutions

As an interface standard that's dominating the market for over two decades, PCIe remains the top choice for internal high-speed expansion across various applications. A PCIe switch plays a crucial role in connecting multiple PCIe endpoints to a single root complex. Beyond implementing standard layered PCIe functionality in its upstream and downstream ports, a PCIe switch must also handle routing, lane multiplexing, traffic management, security and isolation features for virtualization and more.

In collaboration with a leading semiconductor company, we verified multiple generations of PCIe switches, leveraging our deep expertise in the PCIe protocol and our experience with Cadence PCIe VIP and the TripleCheck Test Suite. In this note we summarize the key challenges we encountered and the strategies we used to overcome them.

Challenges

Compliance Testing of PCIe Switch Ports

Since the PCIe switch was our customer's in-house development, ensuring compliance of its ports with PCIe specifications was of critical importance and had to be checked thoroughly. This was particularly complex due to numerous features in all three layers of the PCIe protocol: Physical, Data Link and Transaction Layers. The Physical Layer posed the greatest challenge, with its vast number of rules governing the Link Training and Status State Machine, 8b/10b and 128b/130b encoding, scrambling, SerDes, and more.

System flows

While the PCIe specification defines the necessary rules that make a component PCIe compliant, there are many scenarios that can't be directly referenced in the specification, but where real bugs may arise. These hidden bugs, if not discovered and fixed, can lead to different issues, from performance deterioration to fatal system failures.

Performance and QoS

With multiple PCIe switch ports potentially operating at different speeds, handling various traffic kinds, QoS levels, and ordering rules, ensuring optimal throughput and latency from any source to any destination and for any traffic flow was a significant challenge for the verification team.

Features under development

For some switch generations, we had to prepare verification for features still in the proposal stage for a new PCIe specification version. Often these features were getting redefined, making it difficult to finalize verification development.

Solutions and Approaches

This section outlines the methodologies and advanced techniques our team employs to address the complex challenges presented by PCIe switch verification, ensuring robust performance and compliance with industry standards.

Leveraging the TripleCheck Test Suite

For verifying PCIe switch port compliance, we used Cadence's TripleCheck Test Suite as a foundation. While it offers extensive compliance tests, understanding its limitations is crucial. We conducted a thorough analysis to determine which aspects were covered and which required independent verification. Our expertise in configuring and utilizing the suite allowed us to maximize its effectiveness.

Deep Protocol Knowledge and Understanding of Real-World Usage

To address system flow and performance challenges, we focused on identifying potential conflicting features that could lead to unexpected behavior. After identifying these and with thoroughly understanding real-world use cases, we implemented comprehensive test flows that covered all variations of such scenarios. Our performance measurements and identification of the bottlenecks provided valuable feedback to the design team, ultimately leading to exceptional switch performance.

Flexible Verification Framework

To accommodate features still not finally specified, we had to develop a highly flexible while still robust framework that allowed us to quickly adapt to evolving specification changes. This approach enabled our customer to achieve a short time-to-market for their products.