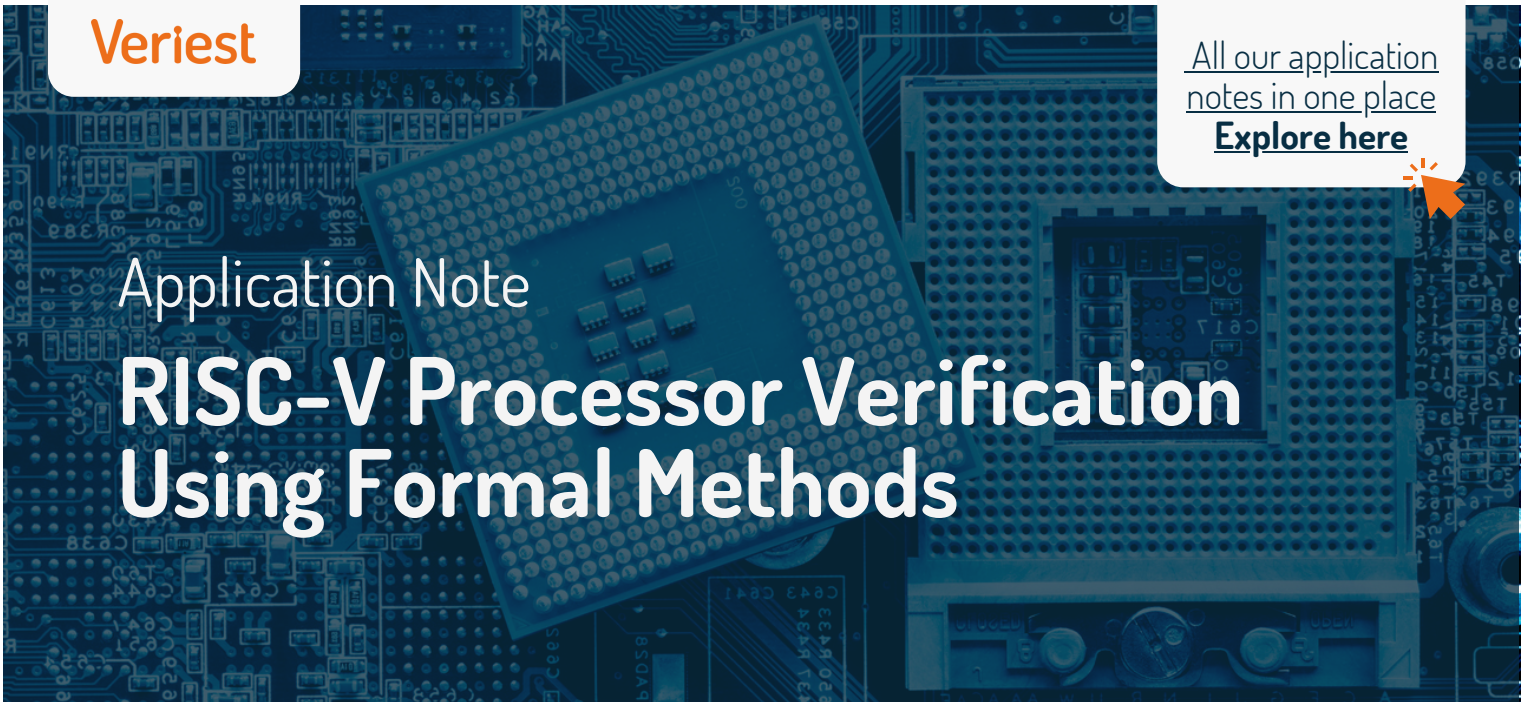
Veriest



All our application notes in one place **Explore here**

Application Note

RISC-V Processor Verification Using Formal Methods

Challenges

- Need to ensure 100% compliance with the RISC-V specification
- Complex pipeline interactions create hard-to-find corner cases
- Difficult to achieve coverage closure with traditional simulation methods
- Custom extensions require rigorous verification of interaction with base ISA
- Time-to-market pressures demand efficient verification solutions

Veriest Solution

Veriest has implemented a comprehensive formal verification strategy

- Expertise in RISC-V architecture
- Experience with RISC-V ISA verification, including use of standard Formal packages
- Experience with RISC-V Memory Management
- Developed “Hook Free” Verification Methodology
  - effective for processors with advanced features, such as complex pipelines, out-of-order execution, etc.
  - implemented on multiple RISC-V cores
- Modular structure for easy addition of custom instructions
- Experience in Formal Verification of non-ISA blocks, which are also part of any RISC-V processor
- Experience in C2RTL tools, for Formal Verification of math and datapath blocks within the processor

Results

- Enhanced confidence in design correctness
- Complete verification of custom extensions
- Reusable formal environment for future projects
- Streamlined regression suite based on formal results