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Application Note

NoC Design & Verification

In high-performance computing, reliable and efficient Network-on-Chip (NoC) solutions are essential for handling significant data rates, achieving optimal latency, and meeting demanding performance requirements. In collaboration with a leading automotive semiconductor company, we undertook a NoC design and verification project, leveraging our experience with the Arteris FlexNoC tool to deliver a robust, high-throughput NoC solution. This note outlines the challenges encountered and the solutions we developed to address them.

Design Challenges

Diverse Network Topologies

Designing interconnect solutions for varied network topologies posed complexity in ensuring consistent performance across all nodes. Maintaining low latency while supporting different topological configurations required precise adjustments and optimizations.

Quality of Service (QoS) and Data Handling

Efficient data handling and QoS management were crucial to prioritize specific data streams, especially in applications where certain data must take precedence. This required implementing dedicated buffers and QoS policies to manage priorities effectively.

Error Handling and Fault Tolerance

Robust error-handling mechanisms were needed to manage various error scenarios, such as timeouts, slave errors, decoding errors, and parity errors. Ensuring resilience against these faults while maintaining system performance was essential for the system's reliability.

Observability

Proactive monitoring and debugging techniques were used to enable real-time tracking of key system parameters, such as traffic, latency and resource usage. By collecting detailed performance data, it allowed for faster debugging, pinpointing bottlenecks, and improving overall system reliability.

Verification Challenges

Connectivity and Performance Validation

Ensuring connectivity between masters, slaves, and multiple NoCs in complex configurations required rigorous verification. We employed both formal and functional methods, using generic latency and performance monitors to validate that the design met performance and connectivity requirements.

Functional Safety Features

Verifying all safety features independently - without relying solely on vendor support - was a priority to ensure compliance with reliability standards. This approach enabled us to address system reliability requirements, strengthening the verification process.

Solutions and Approaches

Advanced Tool Utilization and Customization

We leveraged Arteris's FlexNoC tool to configure buffers, QoS management, observability features, and fault tolerance mechanisms. The Physical Topology Editor was used for efficient module placement, while firewalls and exclusive access features enhanced data security and control.

Automated Regression Testing and Comprehensive End-to-End Verification

To streamline the verification process, we developed a fully automated regression suite, enabling rapid and efficient testing of networks with multiple NoCs. This approach allowed us to perform initial comprehensive testing within weeks, significantly accelerating project-to-project migration. Beyond automation, we conducted complete end-to-end testing of all data paths, integrating real masters and slaves wherever applicable. For NoC network testing, we utilized active master and slave VIPs, ensuring robust validation of network behavior and functionality. This combination of automation and thorough functional testing provided a seamless and reliable verification framework.

Performance Testing in UVM Environments

Leveraging FlexNoC tools, we effectively generated UVM environments to model latency and performance requirements. While FlexNoC FlexExplorer provides a solid foundation for performance analysis, especially in single NoC setups, our expertise lies in complementing it with tailored UVM-based testing techniques. For multi-NoC solutions and scenarios requiring fine-grained traffic configurations, we implemented performance testing directly in UVM, mimicking real traffic flows with high accuracy. Additionally, our environment integrates real masters and slaves where applicable, enabling comprehensive end-to-end testing. This hybrid approach ensures we extract the best from available tools while enhancing them with custom methodologies for superior NoC verification results.

Error Scenario Testing and Recovery

Comprehensive error scenario testing covered various faults, including ECC errors and recovery mechanisms. This validation ensured the system could recover from faults effectively without compromising data integrity or performance.

Integration of NoC network in the chip

The NoC-to-NoC integration and level 0 testing were primarily conducted using a formal connectivity tool, with our team contributing to specific aspects of the process. For in-house components connected to the NoC, such as decoders and arbiters, we utilized Jasper to ensure their functionality and reliability. This combination of formal tools and targeted testing ensured robust integration of the NoC network into the chip design.